

METHODS TO MAKE DIFFRACTIVE OPTICAL ELEMENTS

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FIELD OF INVENTION

[0001] This invention relates to a method for making a diffractive optical element (DOE) using complementary metal oxide semiconductor (CMOS) processes.

DESCRIPTION OF RELATED ART

[0002] Modern optical systems often make use of diffractive optical elements (DOEs). For example, a DOE lens can be used to focus a laser light into an optical fiber. DOEs operate by modifying the phase of light interacting with the element either in transmission or by reflection. DOEs are formed by patterning phase shifting materials into an appropriate lens.

SUMMARY

[0003] In one embodiment of the invention, a method for forming a diffractive lens includes forming an etch stop layer on a first surface of a silicon substrate, forming a diffractive optical element above the etch stop layer, forming a planarization layer covering the diffractive optical element, planarizing the planarization layer, forming a bonding layer on the planarization layer, bonding a transparent substrate on the bonding layer, and etching a second surface of the silicon substrate to the etch stop layer to remove a portion of the silicon substrate opposite the diffractive optical element, wherein the remaining portion of the silicon substrate forms a bonding ring.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Fig. 1 is a flowchart of a method for making a diffractive optical element (DOE) on a transparent substrate in one embodiment of the invention.

[0005] Figs. 2A, 2B, 2C, 2D, and 2E illustrate the resulting structures formed using the method of Fig. 1 in one embodiment of the invention.

[0006] Fig. 3 is a flowchart of a method for making a DOE on a transparent substrate in another embodiment of the invention.

[0007] Fig. 4 illustrates the resulting structure formed using the method of Fig. 3 in one embodiment of the invention.

[0008] Fig. 5 is a flowchart of a method for making a DOE on a silicon-on-insulator (SOI) substrate in another embodiment of the invention.

[0009] Figs. 6A, 6B, 6C, 6D, 6E, 6F, and 6G illustrate the resulting structures formed using the method of Fig. 5 in one embodiment of the invention.

[0010] Fig. 7 is a flowchart of a method for making a DOE on a silicon substrate and transferring the DOE to a transparent substrate in another embodiment of the invention.

[0011] Figs. 8A, 8B, 8C, 8D, 8E, 8F, and 8G illustrate the resulting structures formed using the method of Fig. 7 in one embodiment of the invention.

[0012] Fig. 9 is a flowchart of a method for making a DOE by transferring a pattern of the DOE from a silicon substrate to a transparent substrate in another embodiment of the invention.

[0013] Figs. 10A, 10B, 10C, and 10D illustrate the resulting structures formed using the method of Fig. 9 in one embodiment of the invention.

[0014] Use of the same reference symbols in different figures indicates similar or identical items. The cross-sectional figures are not drawn to scale and are only for illustrative purposes.

DETAILED DESCRIPTION

[0015] A diffractive optical element (DOE) can be fabricated by forming multilayer materials of amorphous silicon and silicon dioxide supported on a silicon substrate and successively patterning the multilayer materials to form the DOE. Such a DOE takes advantage of the high refractive index of the silicon, the alternating etch stop layers in the multilayer materials, and the precision masking offered by complementary metal oxide semiconductor (CMOS) fabs. Such a DOE is well suited for long wavelengths where the silicon substrate is transparent. Due to high absorption of the silicon substrate in the near infrared for

wavelengths below 1 micron (μm), such a DOE cannot be applied to shorter wavelengths such as 850 and 990 nanometer (nm) generated by some lasers.

[0016] Fig. 1 is a flowchart of a method 10 to form a DOE on a transparent wafer in one embodiment of the invention. Method 10 is hereafter explained in reference to Figs. 2A to 2E.

[0017] In step 12, as shown in Fig. 2A, an opaque coating 32 is formed on the topside of a transparent substrate 34. Opaque coating 32 is applied to transparent substrate 34 so semiconductor equipment using optical sensors can detect and handle transparent substrate 34. Opaque coating 32 is only shown in Fig. 2A. Transparent substrate 34 is transmissive to a wavelength of interest (e.g., selected from infrared to ultraviolet) if a percentage of the incident light specified by the application is transmitted through the substrate (e.g., at least 10% for most communication applications). Transparent substrate 34 can be quartz, sodium borosilicate glass (e.g., Pyrex[®]), sapphire, or fuse silica. Opaque coating 32 can be amorphous silicon ($\alpha\text{-Si}$) deposited by low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). Amorphous silicon coating 32 is typically more than $0.5\ \mu\text{m}$ thick.

[0018] In step 14, as shown in Fig. 2A, an antireflective (AR) coating 36 is optionally formed on the backside of transparent substrate 34. AR coating 36 reduces reflection as light travels between a DOE 50 (Fig. 2B) and transparent substrate 34.

[0019] Those skilled in the art understand the choice of the AR coating material depends on the refractive index of the incoming medium, the exit medium, and the AR coating material. The ideal AR coating material has a refractive index that is the geometric mean of the incoming medium and the exit medium. The ideal AR coating thickness is equal to a quarter of the wavelength of the light in the AR coating medium. In one embodiment, AR coating 36 is sandwiched between Pyrex[®] and silicon. Hence, the ideal refractive index is calculated as follows: $\text{sqrt}(1.5 * 3.5) = 2.29$, where 1.5 and 3.5 are the refractive indices of Pyrex[®] and silicon respectively. Thus, titanium dioxide (TiO_2) is selected as the AR material because it has a reflective index of 2.2 that is close to the ideal value of 2.29. The thickness of the TiO_2 AR coating 36 for 990 nm operation is then calculated as follows: $990\ \text{nm} / 4 / 2.2 = 112.5\ \text{nm}$. Those skilled in the art understand that the refractive index and the thickness of AR

coating 36 can be adjusted accordingly. TiO₂ AR coating 36 can be deposited by electron beam (e-beam) evaporation.

[0020] In step 16, as shown in Fig. 2B, a DOE 50 is formed on AR coating 36. DOE 50 includes a stack of phase shifting layers patterned to form the desired diffractive lens. Adjacent phase shifting layers in the stack are separated by an etch stop layer. The phase shifting layers can be amorphous silicon (α -Si) and the etch stop layers can be silicon dioxide (SiO₂). Alternatively, the phase shifting layers can be silicon nitride (Si₃N₄) instead of amorphous silicon.

[0021] The DOE layers can be grown by PECVD. The thicknesses of the amorphous silicon and the oxide layers depend on the wavelength of interest, the number of the layers, and the refractive index of the materials. The total phase shift for light through the DOE stack compared to phase shift going through the air should be an integral multiple of 2π . To take advantage of the high refractive index of silicon, the lower index oxide layer is minimized to about 50 Å. This thickness was experimentally determined to be an effective etch stop layer. Hence, for a typical DOE with 8 interleaving layers of amorphous silicon and oxide layer operating at 990 nm, the total phase shift due to the eight oxide etch stop layers is calculated as follows:

$$\begin{aligned} & (R_{Iox} - R_{IAir}) * 2\pi * (5 \text{ nm} / 990 \text{ nm}) * 8 \\ &= (1.45 - 1) * 2\pi * (5 \text{ nm} / 990 \text{ nm}) * 8 \\ &= 0.1142. \end{aligned}$$

R_{Iox} and R_{IAir} are the refractive indices of oxide etch stop layer and air, respectively. The values 1.45 and 1 are the refractive indices of the oxide layer and the air, respectively. The total phase shift due to the eight amorphous silicon layer is:

$$(R_{Isi} - R_{IAir}) * 2\pi * (t / 990 \text{ nm}) * 8.$$

R_{Isi} is the refractive index of the amorphous silicon layer and t is the thickness of that layer. To achieve the desired phase shift through the DOE stack, each of the amorphous silicon layer thickness is calculated as follows:

$$2\pi - 0.1142 = (R_{Isi} - R_{IAir}) * 2\pi * (t / 990 \text{ nm}) * 8, \text{ or}$$

$$t = (2\pi - 0.1142) * 990 \text{ nm} / [(RI_{Si} - RI_{Air}) * 2\pi * 8]$$

$$t = (2\pi - 0.1142) * 990 \text{ nm} / [(3.5 - 1) * 2\pi * 8]$$

$$t = 48.6 \text{ nm}.$$

The value 3.5 is the refractive index of the amorphous silicon layer.

[0022] Once the stack is formed, the top amorphous silicon layer is masked by photoresist and then etched using the oxide layer to stop the etching. After the silicon is etched, the etch chemistry is changed and the oxide layer is etched using the next silicon layer to stop the etching. Each successive layer is masked and etched to form the desired diffractive lens.

[0023] In one embodiment, DOE 50 is a bifocal diffractive lens that converts laser light into a small angle distribution that is spread uniformly throughout a volume. The volume's dimensions are large relative to the size of the input face of an optical fiber so the components can easily align. The bifocal diffractive lens has a surface with ridges that provide two focal lengths f_1 and f_2 . A design process for the bifocal diffractive lens can begin with determining a first phase function that defines a surface contour for a conventional diffractive lens having focal length f_1 . Any conventional techniques for diffractive lens design can be used. In particular, commercial software such as GLAD from Applied Optics Research, Inc. or DIFFRACT from MM Research, Inc. can analyze the phase functions of diffractive elements. A second phase function is similarly generated, wherein the second phase function is such that if the second phase function were multiplexed together with the first phase function, the combination would provide a diffractive lens having the second focal length f_2 . The second phase function is then scaled so as to provide a partially efficient diffractive lens that focuses a percentage (e.g., 50%) of the incident light but passes the remainder (e.g., 50%) of the incident light unperturbed. The first phase function and the scaled second phase function are multiplexed together to form a final bifocal lens design.

[0024] In another embodiment, DOE 50 is a hybrid diffractive/refractive element. The hybrid diffractive/refractive element spreads the light over a volume to expand the alignment tolerance for an optical fiber as described above. The hybrid diffractive/refractive lens has at least one surface with a curvature for one focal length, e.g., f_2 . Further, diffractive features of a partially efficient diffractive lens are superimposed on one or both surfaces of the hybrid

diffractive/refractive lens so that the combination provides two focal lengths f_1 and f_2 for separate fractions of the incidence light.

[0025] In step 18, as shown in Fig. 2B, an AR coating 51 is optionally formed over DOE 50. The refractive index and thickness of AR coating material 51 can be selected as described above. AR coating 51 can be silicon nitride (Si_3N_4). Thin film silicon nitride material can have a range of refractive index depending on deposition conditions. Nitride AR coating 51, with a refractive index of 1.9, can be deposited by e-beam evaporation and is typically 130 nm thick for 990 nm wavelength. The use of e-beam evaporation provides a non-conformal coating which is more desirable on the grating surface. AR coating 51 is only illustrated in Fig. 2B.

[0026] In step 20, as shown in Figs. 2C and 2D, a silicon substrate 62 is processed to form a bonding ring 62A. A barrier layer 60 is formed on silicon substrate 62. Barrier layer 60 separates any metal from reacting with silicon substrate 62 so that metal silicide will not form in high temperature operations later on. Barrier layer 60 can be silicon nitride (Si_3N_4). Nitride barrier layer 60 can be deposited by PECVD and is typically 0.5 μm thick. Bonding pads 64 are then formed on barrier layer 60. Bonding pads 64 can be formed by patterning a liftoff mask, depositing a metal, and lifting off the mask with the metal. Metal bonding pads 64 can be titanium-platinum-gold (TiPtAu) sequence deposited by e-beam evaporation or sputtering. Titanium has a typical thickness of 50 nm, platinum has a typical thickness of 150 nm, and gold has a typical thickness of 50 nm. A photoresist 66 is then spun, exposed, and developed on barrier layer 60 to form an etch window 67. Portions of barrier layer 60 and silicon substrate 62 exposed by etch window 67 are etched away to form a bonding ring 62A. Barrier layer 60 and silicon substrate 62 can be etched using deep reactive ion etching (DRIE). Photoresist 66 is then stripped away.

[0027] In step 22, as shown in Fig. 2D, bonding ring 62A is bonded to transparent substrate 34 to form a lid 80. If transparent substrate 34 is sodium borosilicate glass, bonding ring 62A can be bonded to transparent substrate 34 by an anodic bond. If transparent substrate 34 is quartz or sapphire, an adhesive bond can be used. Alternatively, a hydrofluoric acid (HF) bond can also be used. In HF bonding, two clean surfaces that are pressed together can be joined by dispensing a small amount of HF between the two surfaces. The HF will fill in the gap between the joining pieces by capillary action. When the HF dries up, the two pieces will be joined permanently. Alternatively, a glass frit bond can be used. In glass frit

bonding, a fine powder of glass is dispensed between the two joining pieces and heated above the glass reflow temperature during the joining process. This temperature depends on the selected glass frit material and is typically above 250° C.

[0028] In step 24, as shown in Fig. 2E, lid 80 is bonded to a submount 82 to complete a microelectronic package 84. Lid 80 and submount 82 can be bonded by solder. Submount 82 can include a light source 86 (e.g., a vertical cavity surface emitting laser (VCSEL)). Submount 82 can also include other active and passive circuitry 88.

[0029] Fig. 3 is a flowchart of a method 90 to form a DOE on a transparent wafer in another embodiment of the invention. Method 90 follows steps 12 to 18 of method 10 in Fig. 1. Step 18 is then followed by step 26 and is hereafter explained in reference to Fig. 4.

[0030] In step 26, as shown in Fig. 4, transparent substrate 34 with DOE 50 is mounted to a submount 92 with a silicone material 94. Submount 92 can include a light source 96 (e.g., a VCSEL). Submount 82 can also include other active and passive circuitry 98.

[0031] Fig. 5 is a flowchart of a method 100 to form a DOE on a silicon-on-insulator (SOI) substrate in another embodiment of the invention. Method 100 is hereafter explained in reference to Figs. 6A to 6G.

[0032] In step 104, as shown in Fig. 6A, DOE 50 is formed on an SOI substrate 142. SOI substrate 142 includes a silicon device layer 144, an oxide insulator layer 146, and a silicon handle layer 148. Silicon device layer 144 is typically less than 20 μm thick, which makes it transmissive to wavelengths of 850 and 990 nm. Oxide insulator layer 146 is later used as an etch stop when silicon handle layer 148 is etched to form a bonding ring 148A (Fig. 6E). In one embodiment, SOI substrate 142 further includes a silicon nitride layer 145 (shown only in Fig. 6A) between device layer 144 and oxide insulator layer 146. Such a SOI substrate 142 can be formed by bonding an oxidized wafer with a wafer that is coated with silicon nitride. After the bonding, the wafer with silicon nitride can be grind and lapped thin to form device layer 144. Using such a SOI substrate 142 would eliminate step 128 described later.

[0033] DOE 50 is formed as described above in method 10 of Fig. 1 but with the following modification. In method 10, the phase shift is due to different speed of light travelling in DOE 50 and air. In this embodiment, the phase shift is due to different speed of light travelling in DOE 50 and oxide planarization layer 160 (Fig. 6C). Since oxide planarization

layer 160 has a refractive index equal or similar to the etch stop oxide in DOE 50, the amorphous silicon thickness is calculated as follows: $(990 \text{ nm} / [(8 * (3.5 - 1.45))]) = 60.37 \text{ nm}$. The total DOE stack thickness is calculated as follows: $[990 \text{ nm} / (3.5 - 1.45) + 5 \text{ nm}] * 8 = 523 \text{ nm}$.

[0034] In step 106, as shown in Fig. 6B, an AR coating 150 is optionally formed over DOE 50. The material and the thickness of AR coating 150 are selected as described above. AR coating 150 can be titanium dioxide (TiO_2). TiO_2 AR coating 150 can be deposited by e-beam evaporation and is typically 112.5 nm thick for 990 nm wavelength. AR coating 150 is only illustrated in Fig. 6B.

[0035] In step 108, as shown in Fig. 6C, a planarization layer 160 is formed over device layer 144 and DOE 50, and then planarized if a flat top surface on the resulting structure is desired. Planarization layer 160 can be silicon dioxide (SiO_2) formed by PECVD. Oxide planarization layer 160 is typically 0.3 μm thicker than DOE 50 so it can be polished by chemical mechanical polishing (CMP) to a flatness of better than 200 angstroms (\AA). In one embodiment for 990 nm wavelength, DOE 50 has a typical thickness of 523 nm. Thus, oxide planarization layer 160 has a typical thickness of 823 nm.

[0036] In step 110, as shown in Fig. 6D, a barrier layer 170 is formed on the backside of SOI substrate 142. Barrier layer 170 can be silicon dioxide (SiO_2). Oxide barrier layer 170 can be deposited by PECVD and is typically 0.5 μm thick.

[0037] In step 112, as shown in Fig. 6D, bonding pads 172 are formed on barrier layer 170. Bonding pads 172 can be titanium-platinum-gold (TiPtAu) sequence deposited by e-beam evaporation or sputtering and patterned by a liftoff mask. Titanium has a typical thickness of 50 nm, platinum has a typical thickness of 150 nm, and gold has a typical thickness of 50 nm.

[0038] In step 114, as shown in Fig. 6D, an etch mask layer 174 is formed over barrier layer 170 and bonding pads 172. If a wet etch is to be used, etch mask layer 174 can be silicon nitride (Si_3N_4) deposited by PECVD. If a dry etch is to be used, etch mask layer 174 can be a photoresist that is spun on.

[0039] In step 116, as shown in Fig. 6E, etch mask layer 174 is patterned to form part of an etch window 176. If etch mask layer 174 is nitride, it can be patterned by spinning on a photoresist, exposing the photoresist, developing the photoresist, and etching the nitride. If

etch mask layer 174 is a photoresist, it can be patterned by exposing and developing the photoresist.

[0040] In step 118, as shown in Fig. 6E, barrier layer 170 is patterned using etch mask layer 174 to form part of etch window 176.

[0041] In step 120, as shown in Fig. 6E, a portion of silicon handle layer 148 located opposite of DOE 50 and exposed by etch window 176 is etched down to oxide insulator layer 146, which acts as an etch stop to form a bonding ring 148A. If etch mask layer 174 is nitride, then silicon handle layer 148 can be etched with a potassium hydroxide (KOH) solution. If etch mask layer 174 is a photoresist, then silicon handle layer 148 can be etched using DRIE.

[0042] In step 122, as shown in Figs. 6E and 6F, the remaining etch mask layer 174 is etched away.

[0043] In step 124, as shown in Figs. 6E and 6F, a portion of oxide insulator layer 146 opposite DOE 50 is etched away. Oxide insulator layer 146 can be etched away using hydrofluoric acid (HF).

[0044] In step 126, as shown in Fig. 6G, an AR coating 190 is optionally formed on planarization layer 160. The material and the thickness of AR coating 190 are selected as described above. AR coating 190 can be magnesium fluoride (MgF_2). MgF_2 AR coating 190 can be deposited by e-beam evaporation and is typically 179.3 nm thick for 990 nm wavelength.

[0045] In step 128, as shown in Fig. 6G, an AR coating 192 is optionally formed on silicon device layer 142 opposite DOE 50. The material and thickness of AR coating 192 are selected as described above. AR coating 192 can be silicon nitride (Si_3N_4). Nitride AR coating 192 can be deposited by e-beam evaporation through a shadow mask and is typically 132.3 nm for 990 nm wavelength. The shadow mask can be a chem-etched metal foil. The evaporated silicon nitride from the source will pass through the holes in the mask and deposit onto the wafer. This mask is normally mechanically aligned and placed close to the wafer. Note that materials such as silicon nitride and amorphous silicon have a range of refractive indices that can be adjusted by process parameter. Those skilled in the art understand how to adjust refractive index by adjusting parameters such as deposition temperature, gas flow

conditions, and pressure. At this point, a lid 194 is formed and can be mounted to a submount to complete a microelectronic package.

[0046] Alternatively, step 128 can be bypassed if a SOI substrate 142 including a silicon nitride layer 145 (Fig. 6A) is used. If such a SOI substrate 142 is used, then silicon nitride layer 145 becomes the AR coating for DOE 50.

[0047] Fig. 7 is a flowchart of a method 200 to form a DOE on a silicon substrate and transferring the DOE onto a transparent substrate in one embodiment of the invention. Method 200 is hereafter explained in reference to Figs. 8A to 8G.

[0048] In step 202, as shown in Fig. 8A, an etch stop layer 240 is formed on the topside of a silicon substrate 242. Etch stop layer 240 can be silicon dioxide (SiO_2). Etch stop layer 240 can be thermally grown or deposited by PECVD and is typically $0.5\ \mu\text{m}$ thick.

[0049] In step 204, as shown in Fig. 8A, an AR coating 244 is optionally formed on etch stop layer 240. The material and the thickness of AR coating 244 are selected as described above. AR coating 244 can be silicon nitride (Si_3N_4). Nitride AR coating 244 can be deposited by PECVD and is typically 132.3 nm thick for 990 nm wavelength.

[0050] In step 208, as shown in Fig. 8A, DOE 50 is formed on AR coating 244. DOE 50 is formed as described above in method 10 of Fig. 1. The thicknesses of DOE layers can be selected as described above.

[0051] In step 210, as shown in Fig. 8B, an AR coating 248 is optionally formed over DOE 50. The material and the thickness of AR coating 248 are selected as described above. AR coating 248 can be titanium dioxide (TiO_2). TiO_2 AR coating 248 can be deposited by e-beam evaporation and is typically 112.5 nm thick for 990 nm wavelength. AR coating 248 is only illustrated in Fig. 8B.

[0052] In step 212, as shown in Fig. 8C, a planarization layer 260 is formed over AR coating 244 and DOE 50, and then planarized. Planarization layer 260 can be silicon dioxide (SiO_2) formed by PECVD. Oxide planarization layer 260 is typically $0.3\ \mu\text{m}$ thicker than DOE 50 so it can be polished by CMP to a flatness of better than 200 Å. Oxide planarization layer 260 is typically $0.8\ \mu\text{m}$ thick.

[0053] In step 214, as shown in Fig. 8C, a bonding layer 262 is formed on planarization layer 260. Bonding layer 262 can be amorphous silicon (α -Si) deposited by PECVD. Silicon bonding layer 262 has a thickness of half a wavelength of interest, or an integral multiple of half a wavelength of interest. Silicon bonding layer 262 is typically 141.4 nm for 990 nm wavelength. Silicon bonding layer 262 improves anodic bonding of an oxide coated silicon substrate to a sodium borosilicate glass (e.g., Pyrex[®]) transparent substrate 270 (Fig. 8D). This layer can be omitted for bonding methods other than anodic bonding.

[0054] In step 216, as shown in Fig. 8D, transparent substrate 270 is bonded to bonding layer 262. Transparent substrate 270 provides the mechanical support for the remaining structure after silicon substrate 242 is later etched away. Transparent substrate 270 is transmissive to a wavelength of interest (e.g., selected from infrared to ultraviolet) if a percentage of the incident light specified by the application is transmitted through the substrate (e.g., at least 10% for most communication applications). Transparent substrate 270 can be quartz, sodium borosilicate glass (e.g., Pyrex[®]), sapphire, or fuse silica. The preferred transparent substrate 270 is sodium borosilicate glass that can be bonded to bonding layer 262 by an anodic bond. Alternatively, an adhesive bond, a HF bond, or a glass frit bond can be used.

[0055] In step 218, as shown in Fig. 8E, a barrier layer 271 is formed on the backside of silicon substrate 242. Barrier layer 271 can be silicon dioxide (SiO_2). Oxide barrier layer 271 can be formed by PECVD and is typically 0.5 μm thick.

[0056] In step 220, as shown in Fig. 8E, bonding pads 272 are formed on barrier layer 271. Bonding pads 272 can be titanium-platinum-gold (TiPtAu) sequence deposited by e-beam evaporation or sputtering and patterned by a liftoff mask. Titanium has a typical thickness of 50 nm, platinum has a typical thickness of 150 nm, and gold has a typical thickness of 50 nm.

[0057] In step 224, as shown in Figs. 8E and 8F, a photoresist layer 274 is formed and patterned to form part of an etch window 278.

[0058] In step 226, as shown in Figs. 8E and 8F, a portion of barrier layer 271 exposed by etch window 278 is etched using photoresist layer 274 to form part of etch window 278.

[0059] In step 228, as shown in Figs. 8E and 8F, a portion of silicon substrate 242 located opposite of DOE 50 and exposed by etch window 278 is etched down to etch stop layer 240 to form a bonding ring 242A. Silicon substrate 242 can be etched by DRIE.

[0060] In step 230, as shown in Figs. 8F and 8G, the remaining photoresist layer 274 is removed chemically by a resist stripper.

[0061] In step 232, as shown in Figs. 8F and 8G, a portion of oxide etch stop layer 240 opposite DOE 50 is etched away to expose a portion of AR coating 244. An optional AR coating of magnesium fluoride (MgF_2) can be e-beam evaporated onto transparent substrate 270. The thickness and refractive index of the MgF_2 can be selected as described above. At this point, a lid 280 is formed and can be mounted to a submount to complete a microelectronic package.

[0062] As an alternative to steps 224 to 232, all of silicon substrate 242 can be etched away to form DOE 50 mounted to transparent substrate 270. This results in a lid 280 without bonding ring 242A.

[0063] Fig. 9 is a flowchart of a method 360 to form a DOE by transferring a pattern for the DOE from a silicon substrate to a transparent substrate in one embodiment of the invention. Method 360 is hereafter explained in reference to Figs. 10A to 10D.

[0064] In step 362, as shown in Fig. 10A, a mold 390 of a DOE is formed on a silicon substrate 392. Mold 390 can be formed similarly as DOE 50 in method 10 of Fig. 1 except it is an inverted image of the DOE instead of the DOE itself. Since the inverted image will be filled with silicon nitride with refractive index of 2.1, the total thickness of this mold 390 will be $990 \text{ nm} / (R_{\text{isin}} - R_{\text{air}}) = 990 \text{ nm} / (2.1 - 1) = 990 \text{ nm}$.

[0065] In step 363, as shown in Fig. 10A, a non-conformal silicon dioxide (SiO_2) layer 393 is formed over mold 390. Non-conformal oxide layer 393 can be deposited by e-beam evaporation. Oxide layer 393 will serve as an etch stop and an AR coating for a nitride DOE 394A (Fig. 10B). The refractive index of oxide layer 393 is typically 1.45. The thickness of oxide layer 393 is selected as described above (e.g., $990 \text{ nm} / 4 / 1.45 = 170.7 \text{ nm}$). As nitride DOE 394A has a refractive index of approximately 2.1, oxide layer 393 with refractive index of 1.45 can be a very effective AR coating material.

[0066] In step 364, as shown in Fig. 10B, a lens layer 394 is formed to cover oxide layer 393 and then planarized. As can be seen, a portion of lens layer 394 that conforms to the pattern of oxide layer 393 form a DOE 394A. Lens layer 394 can be silicon nitride (Si_3N_4) or silicon

dioxide (SiO_2) deposited by PECVD and is typically 1200 nm thick. Lens layer 394 can be planarized by CMP to 900 nm thick.

[0067] In step 365, as shown in Fig. 10B, a transparent substrate 398 is bonded to etch mask layer 394. Transparent substrate 398 is transmissive to a wavelength of interest (e.g., to a wavelength selected from infrared to ultraviolet) if a percentage of the incident light specified by the application is transmitted through the substrate (e.g., at least 10% for most communication applications). Transparent substrate 34 can be quartz, sodium borosilicate glass (e.g., Pyrex[®]), sapphire, or fuse silica. If transparent substrate 398 is sodium borosilicate glass, it can be bonded to a nitride lens layer 394 by an anodic bond. Alternatively, a silicon bonding layer can be formed on an oxide lens layer 394 and a sodium borosilicate glass substrate 398 can be bonded to the silicon bonding layer by an anodic bond.

[0068] In step 366, as shown in Fig. 10B, bonding pads 395 are formed on the backside of silicon substrate 392. Bonding pads 395 can be titanium-platinum-gold (TiPtAu) sequence deposited by e-beam evaporation or sputtering and patterned by a liftoff mask. Titanium has a typical thickness of 50 nm, platinum has a typical thickness of 150 nm, and gold has a typical thickness of 50 nm.

[0069] In step 368, as shown in Fig. 10B, an etch mask layer 396 is formed over the backside of silicon substrate 392 and bonding pads 395. Etch mask layer 396 can be silicon nitride (Si_3N_4) deposited by PECVD.

[0070] In step 372, as shown in Figs. 10B and 10C, etch mask layer 396 is patterned to form an etch window 400.

[0071] In step 374, as shown in Figs. 10C and 10D, a portion of silicon substrate 392 located opposite of DOE 394A and exposed by etch window 400 is etched down to oxide layer 393 to form a bonding ring 392A. Silicon substrate 392 can be etched away by DRIE.

[0072] In step 376, etch mask layer 396 is etched away. At this point, a lid 402 is formed and can be mounted to a submount to complete a microelectronic package.

[0073] Various other adaptations and combinations of features of the embodiments disclosed are within the scope of the invention. Numerous embodiments are encompassed by the following claims.